present claims to the July 1, 1998 priority date, attached to this Request for Reconsideration is a translation of the Japanese priority application.

As the present claims are entitled to the priority date of July 1, 1998, prior to the earliest prior art date (January 27, 1999) of Dibble, Applicant submits that Dibble is not prior art against the present claims.

Second, Watanabe alone does not teach or suggest the claimed subject matter. In each of independent claims 8, 14 and 15, it is required that the adhesive, which is interposed between a surface of the substrate on which an interconnect pattern is formed and a surface of a semiconductor chip in which electrodes are formed, and which has conductive particles dispersed therein, cover all area of lateral (i.e., side) surfaces of the semiconductor chip, which lateral surfaces are substantially perpendicular to the surface of the semiconductor chip on which the electrodes are formed. Applicant respectfully submits that Watanabe does not teach or suggest a semiconductor device, circuit board or electronic instrument in which the adhesive joining the semiconductor chip and the interconnect pattern substrate is made to cover all area of lateral surfaces of the semiconductor chip.

As described at the bottom of page 18 of the present specification, by covering all of the lateral surfaces of the semiconductor chip with an anisotropic conductive material, the semiconductor chip can be protected from mechanical damage. Further, corrosion of the electrodes of the semiconductor chip can be prevented. These benefits are nowhere taught or suggested in Watanabe. In fact, Watanabe describes no reason whatsoever for having the adhesive 18 cover portions of the lateral surfaces of the semiconductor chip. In view of this, one of ordinary skill in the art would have had no motivation to have modified the teachings of Watanabe to make the adhesive cover all of the lateral surfaces of the semiconductor chip, rather than just portions of the lateral surfaces. Thus, nothing in Watanabe would have led one of ordinary skill in the art to the presently claimed invention.

For at least the foregoing reasons, Applicant respectfully submits that Dibble is not prior art and that Watanabe alone neither teaches nor suggests the presently claimed subject matter. Reconsideration and withdrawal of this rejection are respectfully requested.

B. Watanabe in view of Dibble, and further in view of Tsukagoshi

Claim 11 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Watanabe in view of Dibble, and further in view of U.S. Patent No. 5,804,882 (Tsukagoshi). This rejection is respectfully traversed.

First, here again Dibble is not prior art to the present claims.

Second, the Patent Office correctly noted that Watanabe does not teach or suggest that the adhesive is provided to cover the entirety of the interconnect pattern as required in dependent claim 11. The Patent Office turned to the teachings of Tsukagoshi as allegedly suggesting such embodiment.

However, even if the teachings of Watanabe alone and Tsukagoshi were to have been combined, Applicant respectfully submits that the presently claimed invention still would not have been achieved. Specifically, Tsukagoshi fails to remedy the deficiencies of Watanabe discussed above.

Tsukagoshi describes a semiconductor device in which a semiconductor chip 1 having electrodes 2 to thereon is joined to a substrate 4 having circuits 5 and projecting electrodes 7 thereon by way of an adhesive 11 that includes electroconductive particles 12. However, as clearly shown in Figs. 1-4 and 9 of Tsukagoshi, Tsukagoshi does not teach or suggest that the adhesive must be made to cover all area of lateral surfaces of the semiconductor chip. Thus, Tsukagoshi suffers from the same deficiencies as Watanabe discussed above.

For at least the foregoing reasons, Applicant respectfully submits that Dibble is not prior art and that the combined teachings of Watanabe and Tsukagoshi fail to teach or suggest

the presently claimed subject matter. Reconsideration and withdrawal of this rejection are respectfully requested.

C. Watanabe in view of Dibble and further in view of Canning

Claim 12 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Watanabe in view of Dibble and further in view of U.S. Patent No. 5,783,465 (Canning). This rejection is respectfully traversed.

First, here again Dibble is not prior art to the present claims.

Second, the Patent Office acknowledged that Watanabe failed to teach or suggest that the adhesive should include a shading material as required in dependent claim 12. The Patent Office turned to the teachings of Canning as allegedly remedying this deficiency.

Applicant respectfully submits that even if the teachings of Watanabe alone and Canning were to have been combined in the manner alleged in the Office Action, the presently claimed invention still would not have been achieved. That is, Canning also fails to teach or suggest providing an adhesive having conductive particles dispersed therein and being configured to cover all area of lateral surfaces of a semiconductor chip.

Thus, Applicant respectfully submits that Dibble is not prior art and that neither Watanabe nor Canning, taken singly or together, teaches or suggests the presently claimed subject matter. Reconsideration and withdrawal of this rejection are respectfully requested.

II. Rejoinder

Non-elected claims 1, 2, 5-7 and 23 are directed to a method of making the semiconductor device of claim 8, and include all of the limitations of claim 8. Thus, upon allowance of claim 8, the non-elected claims should be rejoined with the application and allowed along with claim 8.

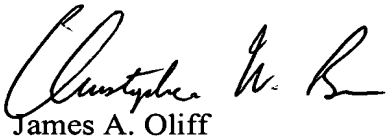
Therefore, upon allowance of claim 8, rejoinder and allowance of presently non-elected claims 1, 2, 5-7 and 23 is respectfully requested.

III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1, 2, 5-8, 11, 12, 14-16 and 21-26 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Christopher W. Brown
Registration No. 38,025

JAO:CWB/wp

Attachment:
English-language Translation of Japanese Priority Document

Date: November 24, 2004

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461